

DERWENT-ACC-NO: 2003-706763

DERWENT-WEEK: 200367

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TITLE: Multi-metal-layer interconnect structure and
method for testing strength of intermetal dielectric
layer - to prevent crack of intermetal dielectric layer

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
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TW 522539 A	March 1, 2003	N/A
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APPLICATION-DATA:

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INT-CL (IPC): H01L021/66, H01L023/52

ABSTRACTED-PUB-NO: TW 522539A

BASIC-ABSTRACT:

NOVELTY - A multi-metal-layer interconnect structure is disposed on a semiconductor substrate having a circuit thereon. The structure comprises: a dielectric layer deposited on the semiconductor substrate; a first metal line layer and a second metal line layer, separately mounted in the dielectric layer, in which the first metal line layer is substantially parallel to the second metal line layer at a clearance d; a plurality of first plugs installed in the dielectric layer, connected to the first metal line layer,

and
electrically connected to the circuit of the semiconductor
substrate; a
plurality of second plugs installed in the dielectric layer,
connected to the
second metal line layer, and electrically connected to the circuit
of the
semiconductor substrate; a third metal line layer and a fourth
metal line layer
located on the first and second metal line layers, and connected to
the first
and second plugs to form a metal dual damascene structure, in which
the third
metal line layer is adjacent to one side of the fourth metal line
layer at an
underneath location larger than $1/2d$ of the clearance between the
first and
second metal line layers, and the third and fourth metal line
layers are still
parallel to each other at a clearance d .

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: MULTI METAL LAYER INTERCONNECT STRUCTURE METHOD TEST
STRENGTH

DIELECTRIC LAYER PREVENT CRACK DIELECTRIC LAYER

DERWENT-CLASS: S01 U11

EPI-CODES: S01-G03; U11-D03C1A; U11-F01A9; U11-F01C;

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